

**15.00 – 16.00 Session 6: DEGRADATION AND PARASITIC EFFECTS**

**An Analytical Model of the RF Impedance Change Due to Solder Joint Cracking**

M. H. Azarian, E. Lando, M. Pecht - CALCE, Univer. of Maryland, USA

**Numerical Simulation of Impedance Discontinuities Resulting from Degradation of Interconnections on Printed Circuit Boards**

P. Manfredi<sup>1</sup>, M. H. Azarian<sup>2</sup>, and F. G. Canavero<sup>1</sup>

<sup>1</sup> Politecnico di Torino, ITALY; <sup>2</sup> CALCE, Univer. of Maryland, USA

**Closed-form Expressions for Modeling Metal Fill Effects in Interconnects**

V. S. Shilimkar, S. G. Gaskill, A. Weisshaar - Oregon State Univ., USA

16.40 – Social event: tour and dinner

**MAY 11- WEDNESDAY**

**9.00 – 10.20 Session 7: MACROMODELING**

**Fast Channel Simulation via Waveform Over-Relaxation**

S. Grivet-Talocia, V. Loggia - Politecnico di Torino, ITALY

**Partitioned Latency Insertion Method (PLIM) with Stability Considerations**

P. Goh<sup>1</sup>, J. E. Schutt-Aine<sup>1</sup>, D. Klokotov<sup>1</sup>, J. Tan<sup>2</sup>, P. Liu<sup>2</sup>, W. Dai<sup>2</sup>, F. Al-Hawari<sup>2</sup> - <sup>1</sup> University of Illinois; <sup>2</sup> Cadence Design Systems, USA.

**Sensitivity Analysis using Data-Driven Parametric Macromodels**

K. Chemmangat, F. Ferranti, L. Knockaert, and T. Dhaene

Ghent University-IBBT, BELGIUM

**Statically constrained nonlinear models with application to IC buffers**

C. Diouf<sup>1</sup>, M. Telescu<sup>1</sup>, N. Tanguy<sup>1</sup>, P. Cloastre<sup>1</sup>, I.S. Stievano<sup>2</sup>, F.G. Canavero<sup>2</sup> - <sup>1</sup> Université Européenne de Bretagne. Université de Brest, CNRS; <sup>2</sup> Politecnico di Torino, ITALY

**10.40-11.40 Session 8: TRANSMISSION LINES AND WAVEGUIDES**

**A Simple Computation of the High-Frequency Per-Unit-Length Resistance Matrix.** F. Broydé and E. Clavelier - Tekcem, FRANCE

**Time Domain Parametric Sensitivity Analysis of Multiconductor Transmission Lines**

D. Spina<sup>1</sup>, F. Ferranti<sup>1</sup>, G. Antonini<sup>2</sup>, T. Dhaene<sup>1</sup>, L. Knockaert<sup>1</sup>

<sup>1</sup> Ghent University-IBBT, BELGIUM; <sup>2</sup> Università dell'Aquila, ITALY

**Wideband Electromagnetic Modeling of Coplanar Waveguides Fabricated in Membrane Technology**

U. Arz<sup>1</sup>, M. Rohland<sup>1,2</sup>, K. Kuhlmann<sup>1</sup>, S. Büttgenbach<sup>2</sup>

<sup>1</sup> Physikalisch-Technische Bundesanstalt, <sup>2</sup> Institut für Mikrotechnik, Braunschweig, GERMANY

11.40 – 12.00 Closing Ceremony.

Organized by:



Università di  
Napoli Federico II  
Italy



Università di  
Cassino  
Italy



Università di Napoli  
Parthenope  
Italy

In collaboration with:



Consorzio  
C.R.E.A.T.E.  
Naples, Italy

Supported by:



Leading Innovation >>>



**SPI 2011**



15<sup>th</sup> IEEE Workshop on

**SIGNAL PROPAGATION ON  
INTERCONNECTS**

Conference Centre "Federico II"

May 8-11, 2011 • Naples • Italy



**PROGRAM**

Sponsored by:



IEEE Components, Packaging and  
Manufacturing Technology Society

Technically co-sponsored by:



IEEE Electromagnetic Compatibility  
Society

[www.spi2011.unina.it](http://www.spi2011.unina.it)

## MAY 8 – SUNDAY

19.00 – Welcome party

## MAY 9 – MONDAY

**10.00 – 10.10 Opening.**

### 10.10 – 11.00 Invited lecture

**Technical and Economical Challenges for Electronic Packaging Engineers:** Moises Cases, *The Cases Group (US)*

### 11.20-12.40 Session 1: EMC ISSUES

**Routing Strategies for Improving Common Mode Filter Performances in High Speed Digital Differential Interconnects**

F. de Paulis, L. Raimondo, D. Di Febo, A. Orlandi  
*University of L'Aquila, ITALY*

**Time domain analysis of a wideband common-mode suppression filter for bent interconnects**

C. Gazda<sup>1</sup>, D. Vande Ginste<sup>1</sup>, H. Rogier<sup>1</sup>, D. De Zutter<sup>1</sup>, and R.-B. Wu<sup>2</sup>  
<sup>1</sup>Ghent University, BELGIUM, <sup>2</sup>National Taiwan Univ. Taipei TAIWAN

**Preventing RFIC interference issues: a modeling methodology for floorplan development and verification of isolation and grounding strategies**

J. Niehof, J. van Sinderen - *NXP Semiconductors, THE NETHERLANDS*

**Crosstalk in VLSI Partially Coupled Interconnect Structures, a Comprehensive Evaluation**

G.Fattah<sup>1</sup>, N. Masoumi<sup>2</sup> - <sup>1</sup>Kerman G.U.T. <sup>2</sup>University of Tehran, IRAN

12.40 – 14.00 lunch

### 14.00 – 14.40 Special Lecture

**On the propagation of electromagnetic signals in wires: 150 years of history:** G. Miano, *University of Naples Federico II, ITALY*

### 14.40 – 16.00 Session 2: MODEL ORDER REDUCTION

**Robust Macromodeling of Frequency Responses with Outliers**

D. Deschrijver, L. Knockaert, T. Dhaene - *Ghent University, BELGIUM*

**A digital filtering approach for Time Domain Vector Fitting**

A. Ubolli<sup>1</sup> and B. Gustavsen<sup>2</sup>  
<sup>1</sup>Norwegian Univ. of Science & Technology, <sup>2</sup>SINTEF - NORWAY

**On the Concretely Passive Realization of Reduced Circuit Models Based on Convex Constrained Positive Real Fractions Identification**

M. de Magistris, M. Nicolazzo - *University of Naples Federico II, ITALY*

**A Novel Algorithm for Optimum Order Estimation of Reduced Order Macromodels**

B. Nouri, M. S. Nakhla, and R. Achar - *Carleton University, CANADA.*

### 16.00 – 16.20 Poster presentation

### 16.20 – 17.40 Poster session

**Crosstalk Modeling in Multiwalled Carbon Nanotubes as Interconnects Using the Compact RC Model**

H. Sheikhsadi<sup>1</sup>, N. Masoumi<sup>2</sup>, A. Hakimi<sup>1</sup>  
<sup>1</sup>Kerman Graduate U.T., <sup>2</sup>University of Tehran, Tehran, IRAN

**Modelling Semiconductor Junctions Including Nonlinear Capacitive Effects using Neural Networks**

P. Gunupudi, P. Tang, Q. J. Zhang and T. Smy  
*Carleton University, Ottawa, CANADA*

**Gradient Resistivity Method for Numerical Evaluation of Anomalous Skin Effect**

A.Tsuchiya<sup>1</sup>, H.Onodera<sup>1,2</sup> - <sup>1</sup>Kyoto Univ.; <sup>2</sup>PESEC, Kyoto Univ., JAPAN

**EMI Filter design using high frequency model of the coupled inductors**

J. L. Kotny, T. Duquesne, N. Idir - *Univ. Lille Nord de France, FRANCE*

**Overshoot and Clock Skew in inverter-interconnect-inverter VLSI systems**

A. Wardzińska, W. Bandurski - *Poznan Univ. of Technology, POLAND*

**Robust Predictability of Parasitic Effects during the Physical Design of RF Products.**

M. Hanssen, H. Gul, Y. Chen, M. Geurts, C. van Dinther, J. Niehof, M.S.-Szalowski, R.Janssen - *NXP Semiconductors, THE NETHERLANDS*

**Efficient Full-wave Broadband Modelling of Interconnects with Graphics Processors**

A.G. Chiariello<sup>1</sup>, A.Maffucci<sup>1</sup>, M. Nicolazzo<sup>2</sup>, S. Ventre<sup>1</sup>, and F. Villone<sup>1</sup> - <sup>1</sup>Univ. di Cassino; <sup>2</sup>Università di Napoli "Federico II", ITALY

18.00 – Social event: tour

## MAY 10 – TUESDAY

### 9.00–10.20 Session 3: SIGNAL AND POWER INTEGRITY ANALYSIS

**Extracting Vectors from Application Traces for Power Integrity Analysis.** M. Olsson<sup>1</sup>, J. Pihl<sup>1</sup>, D. Andersson<sup>1</sup>, P. Larsson-Edefors<sup>2</sup>

<sup>1</sup>Atmel Norway; <sup>2</sup>Chalmers University of Tech., SWEDEN

**Electrical Performance of a Multiport Interposer for Measurements of Dense Via Arrays**

M. Kotzev<sup>1</sup>, Y. H. Kwark<sup>2</sup>, C. Baks<sup>2</sup>, X. Gu<sup>2</sup>, C. Schuster<sup>1</sup>  
<sup>1</sup>TU of Hamburg-Harburg, GERMANY; <sup>2</sup>IBM T.J. Watson R.C., USA.

**Constant-Current Power Transmission Line based Power Delivery Network for Single-Ended Signaling with Reduced Simultaneous Switching Noise**

S. Huh, M. Swaminathan, D. Keezer - *Georgia Institute of Tech., USA.*

**Fast Parametric Pre-Layout Analysis of Signal Integrity for Backplane Interconnects**

R. Rimolo-Donadio<sup>2</sup>, T.-M. Winkel<sup>1</sup>, C. Siviero<sup>1</sup>, D. Kaller<sup>1</sup>, H. Harrer<sup>1</sup>, H.-D. Brüns<sup>2</sup>, C. Schuster<sup>2</sup>

<sup>1</sup>IBM ST Group, GERMANY; <sup>2</sup>TU of Hamburg-Harburg, GERMANY

### 10.40 – 11.20 Tutorial

**Multiphysics Solutions for Silicon-Based High Density Interconnects and Miniaturized Devices with High Performance**

Wen-Yan Yin, *Zhejiang University, Hangzhou, CHINA.*

### 11.20 – 12.40 Session 4: 3-D IC INTERCONNECTS

**Channel Design for Wide System Bandwidth in a TSV based 3D IC**

H. Kim<sup>1</sup>, J. Cho<sup>1</sup>, J. Kim<sup>1</sup>, M. Kim<sup>1</sup>, J. Lee<sup>2</sup>, H. Lee<sup>2</sup>, K. Park<sup>2</sup>, J. Kim<sup>1</sup>, J. S. Pak<sup>1</sup> - <sup>1</sup>KAIST; <sup>2</sup>Hynix Semiconductor Inc., SOUTH KOREA.

**Extraction of Equivalent High Frequency Models for TSV and RDL Interconnects Embedded in Stacks of the 3D Integration Technology**

L. Fourneau<sup>1</sup>, T. Lacrevez<sup>1</sup>, J. Charbonnier<sup>2</sup>, C. Fuchs<sup>2</sup>, A. Farcy<sup>3</sup>, C. Bermond<sup>1</sup>, E. Eid<sup>1</sup>, J. Roullard<sup>1</sup>, B.Flechet<sup>1</sup> - <sup>1</sup>Université de Savoie; <sup>2</sup>CEA-LETI Minatex; <sup>3</sup>STMicroelectronics, FRANCE

**Electrical Behavior of Stacked Microvias Integration Technologies for Multi-gigabits Applications Using 3D Simulation**

C. Chastang<sup>1,3</sup>, C. Gautier<sup>3</sup>, M. Brizoux<sup>2</sup>, A. Grivon<sup>2</sup>, V. Tissier<sup>1</sup>, A. Amedeo<sup>1</sup>, F. Costa<sup>3,4</sup> - <sup>1</sup>THALES Communications; <sup>2</sup>THALES Corporate Services; <sup>3</sup>SATIE CNRS, <sup>4</sup>Université Paris Est, FRANCE

**3D Interconnection Using Butterfly Via for High Speed and RF Package Design**

S. Lee, J.H. Yu, G.W. Kim, J. Kim - *Amkor Technology SOUTH KOREA*

12.40 – 14.00 Lunch

### 14.00 – 15.00 Session 5: INNOVATIVE NANO-INTERCONNECTS

**Electrical Behavior of Carbon Nanotube Through-Silicon Vias**

G. Chiariello<sup>1</sup>, A. Maffucci<sup>1</sup>, G. Miano<sup>2</sup>  
<sup>1</sup>Università di Cassino; <sup>2</sup>Università di Napoli Federico II, ITALY

**Modeling of Carbon Nanotube (CNT) Interconnects**

Wen-Yan Yin<sup>1,2</sup>, Wen-Sheng Zhao<sup>1</sup>  
<sup>1</sup>Zhejiang University; <sup>2</sup>Shanghai Jiao Tong Univ., Shanghai, CHINA

**Impact of Parameters Variability on the Electrical Performance of Carbon Nanotube Interconnects**

I. S. Stievano, P. Manfredi, F. G. Canavero  
*Politecnico di Torino, ITALY*